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FIG. 1 (PRIOR ART)

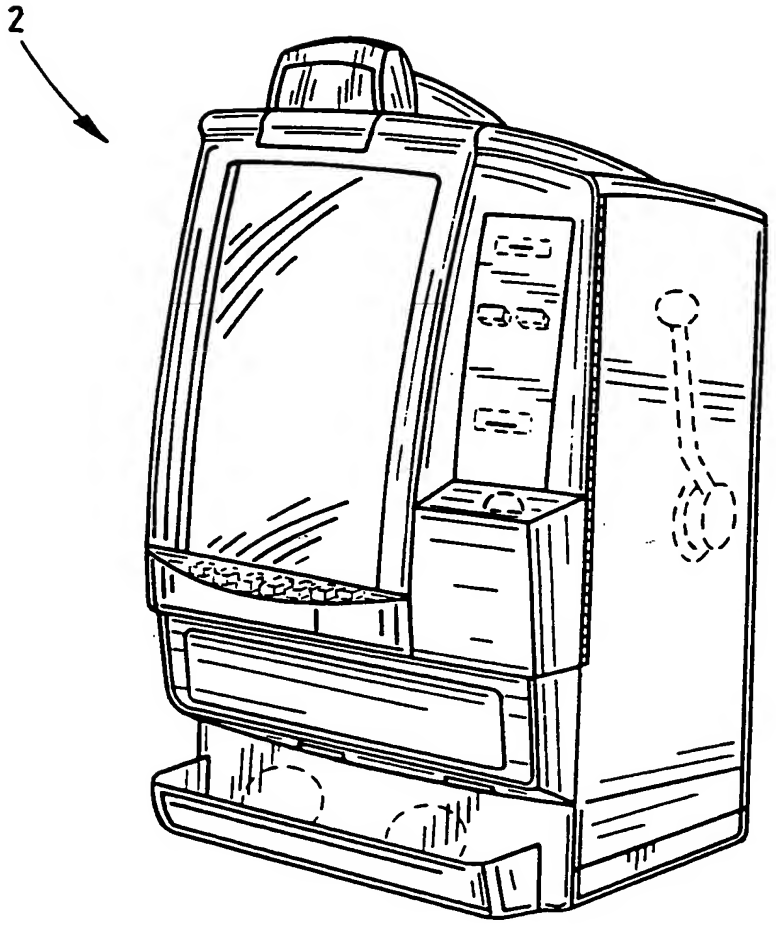
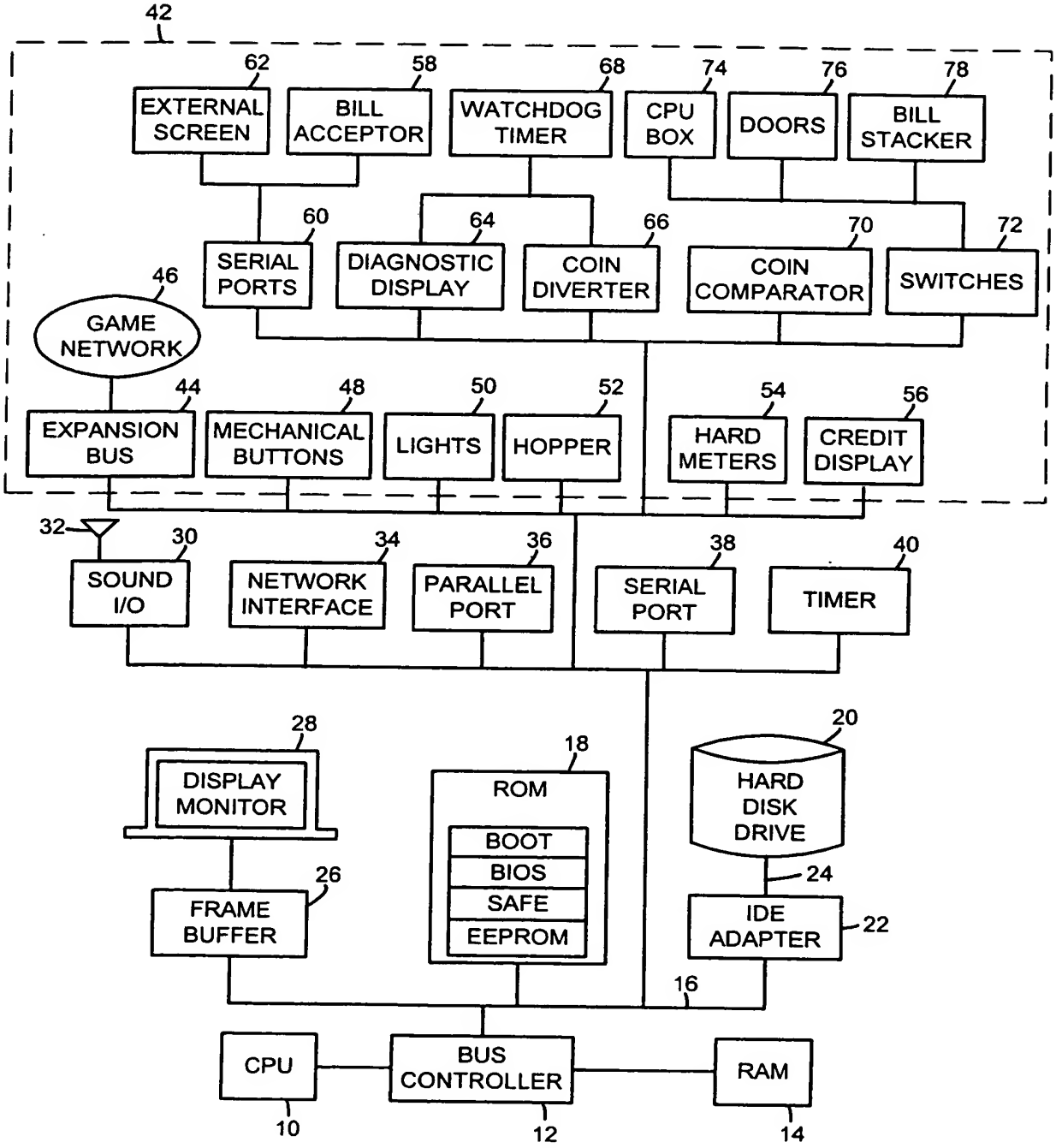


FIG. 2
(PRIOR ART)



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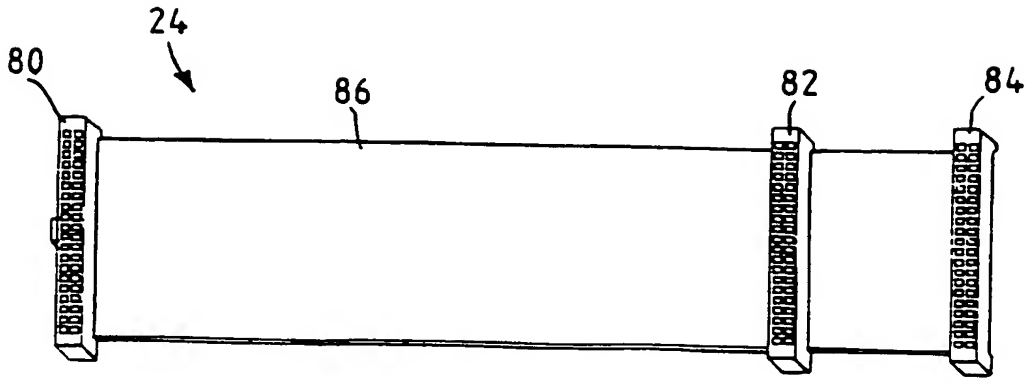

FIG. 3 (PRIOR ART)

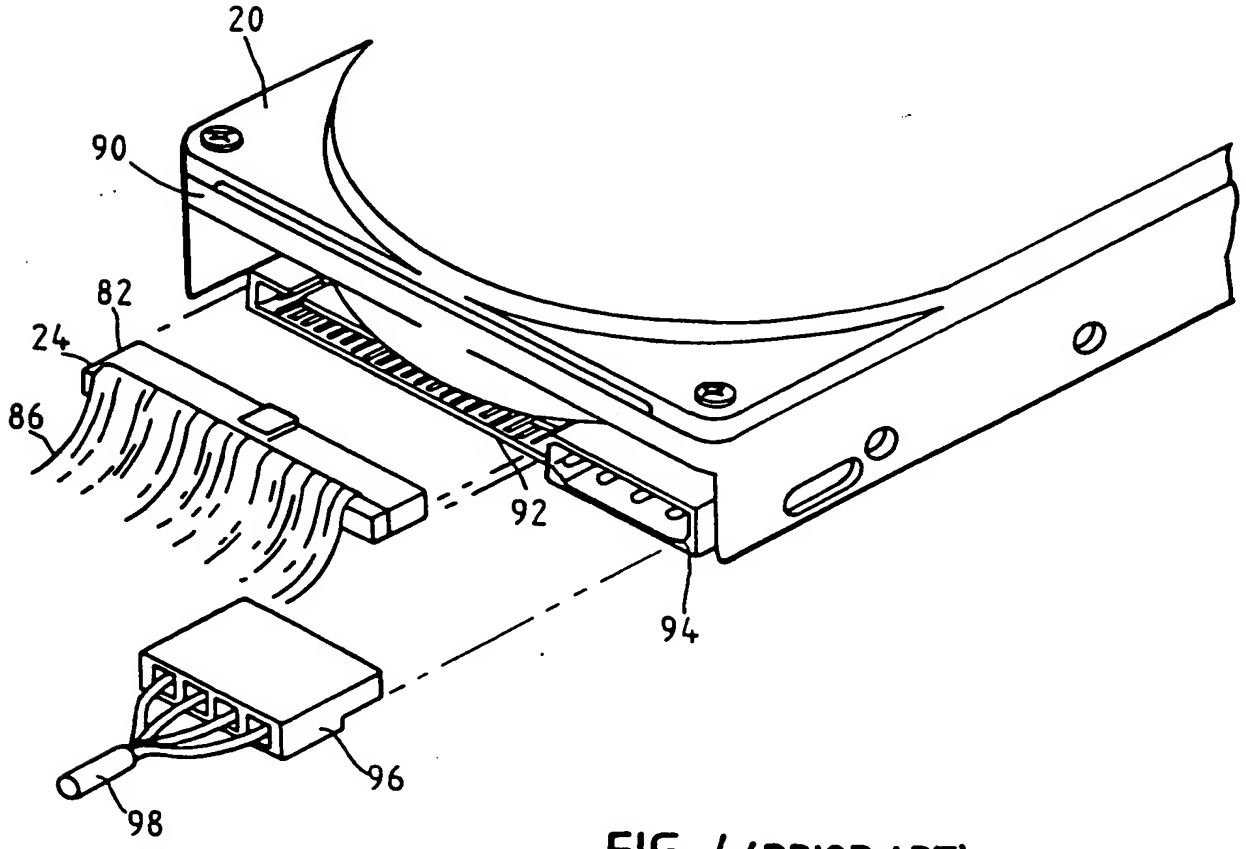

FIG. 4 (PRIOR ART)

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NAME	SOURCE	SIGNAL	PIN	PIN	SIGNAL	SOURCE	NAME
RESET	I	$\overline{\text{RESET}}$	1	2	GROUND		GROUND
DATA BUS BIT 7	I/O	DD7	3	4	DD8	I/O	DATA BUS BIT 8
DATA BUS BIT 6	I/O	DD6	5	6	DD9	I/O	DATA BUS BIT 9
DATA BUS BIT 5	I/O	DD5	7	8	DD10	I/O	DATA BUS BIT 10
DATA BUS BIT 4	I/O	DD4	9	10	DD11	I/O	DATA BUS BIT 11
DATA BUS BIT 3	I/O	DD3	11	12	DD12	I/O	DATA BUS BIT 12
DATA BUS BIT 2	I/O	DD2	13	14	DD13	I/O	DATA BUS BIT 13
DATA BUS BIT 1	I/O	DD1	15	16	DD14	I/O	DATA BUS BIT 14
DATA BUS BIT 0	I/O	DD0	17	18	DD15	I/O	DATA BUS BIT 15
GROUND		GROUND	19	20	N.C.		NO CONNECTION
DMA REQUEST	O	DMARQ	21	22	GROUND		GROUND
I/O WRITE	I	$\overline{\text{DIOW}}$	23	24	GROUND		GROUND
I/O READ	I	$\overline{\text{DIOR}}$	25	26	GROUND		GROUND
I/O CHANNEL READY	O	IORDY	27	28	SPSYNC: CSEL		SPINDLE SYNC or CABLE SELECT
DMA ACKNOWLEDGE	I	DMACK	29	30	GROUND		GROUND
INTERRUPT REQUEST	O	INTRQ	31	32	$\overline{\text{IOCS16}}$	O	16 BIT I/O
ADDRESS BIT 1	I	DA1	33	34	$\overline{\text{PDLAG}}$		PASSED DIAGNOSTIC
ADDRESS BIT 0	I	DA0	35	36	$\overline{\text{DA2}}$	I	ADDRESS BIT 2
CHIP SELECT 0	I	$\overline{\text{CS1FX}}$	37	38	$\overline{\text{CS3FX}}$	I	CHIP SELECT 1
DRIVE ACTIVE/ DRIVE 1 PRESENT	O	$\overline{\text{DASP}}$	39	40	GROUND		GROUND

FIG. 5 (PRIOR ART)

USSN: 10/614,570
Atty. Dkt. #: 29757/SG0042-CON
Applicants: Charles R. Berg, et al.
MARSHALL, GERSTEIN & BORUN LLP 312/ 474-6300
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FIG. 6 (PRIOR ART)

COMMAND NAME	COMMAND CODE
NOP	00h
CFA REQUEST EXTENDED ERROR CODE	03h
DEVICE RESET	08h
READ SECTOR(S)	20h
WRITE SECTOR(S)	30h
CFA WRITE SECTORS WITHOUT ERASE	38h
READ VERIFY SECTOR(S)	40h
SEEK	70h
CFA TRANSLATE SECTOR	87h
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
PACKET	A0h
IDENTIFY PACKET DEVICE	A1h
SERVICE	A2h
SMART	B0h
CFA ERASE SECTORS	C0h
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
READ DMA QUEUED	C7h
READ DMA	C8h
WRITE DMA	CAh
WRITE DMA QUEUED	CCh
CFA WRITE MULTIPLE WITHOUT ERASE	CDh
GET MEDIA STATUS	DAh
MEDIA LOCK	DEh
MEDIA UNLOCK	DFh
STANDBY IMMEDIATE	E0h
IDLE IMMEDIATE	E1h
STANDBY	E2h
IDLE	E3h
READ BUFFER	E4h
CHECK POWER MODE	E5h
SLEEP	E6h
FLUSH CACHE	E7h
WRITE BUFFER	E8h
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
SET FEATURES	EFh
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h
SECURITY FREEZE LOCK	F5h
SECURITY DISABLE PASSWORD	F6h
READ NATIVE MAX ADDRESS	F8h
SET MAX ADDRESS	F9h
VENDOR SPECIFIC	9Ah,C0h-C3h,8xh,F0h,F7h,FAh-FFh
RETIRED	11h-1Fh,71h-7Fh,94h-99h, DBh-DDh,E9h
OBSOLETE	10h,21h-23h,31h-33h,3C,41h, 50h,C9h,CBh,EEh

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IDE command and control register

FIG. 7 (PRIOR ART)

ADDRESS					*NAME AND FUNCTION*	
CS1FX	CS3FX	DA2	DA1	DA0	READ ACCSESS	WRITE ACCSESS
COMMAND REGISTER BLOCK						
1	0	0	0	0	DATA REGISTER	DATA REGISTER
1	0	0	0	1	ERROR REGISTER	FEATURE REGISTER
1	0	0	1	0	SECTOR COUNT REGISTER	SECTOR COUNT REGISTER
1	0	0	1	1	SECTOR NUMBER REGISTER	SECTOR NUMBER REGISTER
					SECTOR NUMBER OR BLOCK	SECTOR NUMBER OR BLOCK
					ADDRESS 0-7	ADDRESS 0-7
1	0	1	0	0	CYLINDER REGISTER 0	CYLINDER REGISTER 0
					CYLINDER 0-7 OR	CYLINDER 0-7 OR
					BLOCK ADDRESS 8-15	BLOCK ADDRESS 8-15
1	0	1	0	1	CYLINDER REGISTER 1	CYLINDER REGISTER 1
					CYLINDER 8-15 OR	CYLINDER 8-15 OR
					BLOCK ADDRESS 16-23	BLOCK ADDRESS 16-23
1	0	1	1	0	DRIVE/HEAD REGISTER	DRIVE/HEAD REGISTER
					DRIVE/HEAD NUMBER OR	DRIVE/HEAD NUMBER OR
					BLOCK ADDRESS 24-27	BLOCK ADDRESS 14-31
1	0	1	1	1	STATUS REGISTER	COMMAND REGISTER
CONTROLREGISTER BLOCK						
0	1	0	0	0	NOT USED	NOT USED
0	1	0	0	1	NOT USED	NOT USED
0	1	0	1	0	NOT USED	NOT USED
0	1	0	1	1	NOT USED	NOT USED
0	1	1	0	0	NOT USED	NOT USED
0	1	1	0	1	NOT USED	NOT USED
0	1	1	1	0	ALTERNATE STATUS REGISTER	CONTROL REGISTER
0	1	1	1	1	ADDRESS REGISTER	NOT USED

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IDE status register

7	6	5	4	3	2	1	0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

FIG. 8 (PRIOR ART)

IDE error register

7	6	5	4	3	2	1	0
BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF

FIG. 9 (PRIOR ART)

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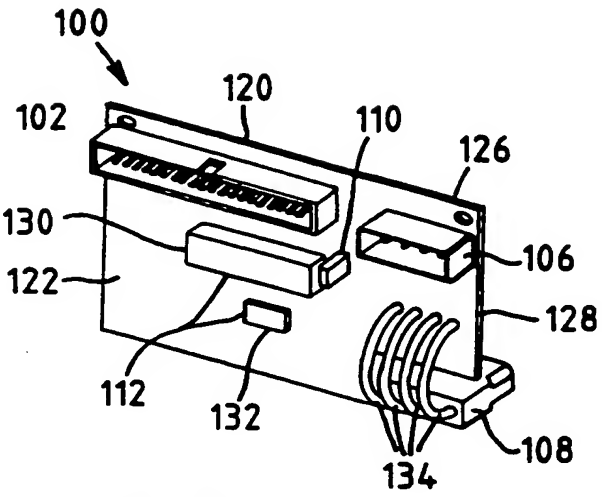

FIG. 10A

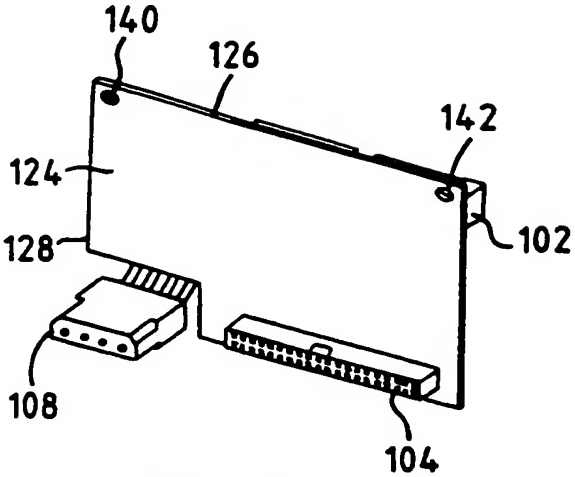

FIG. 10B

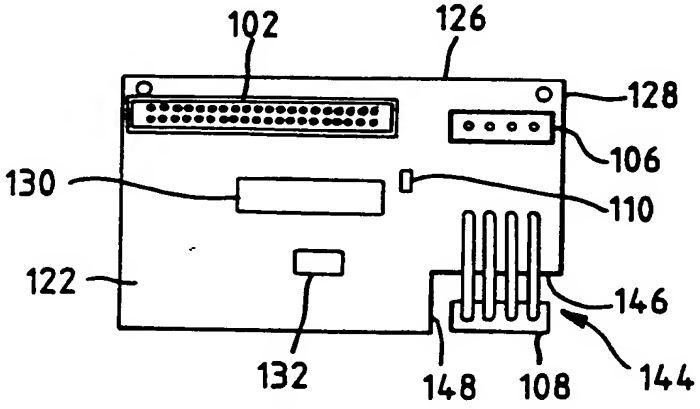

FIG. 10C

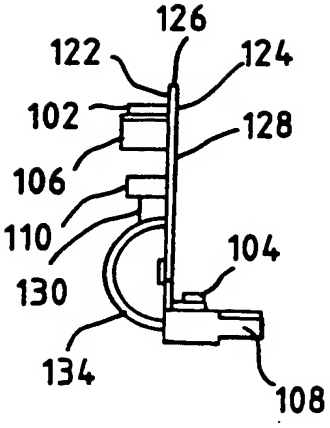

FIG. 10D

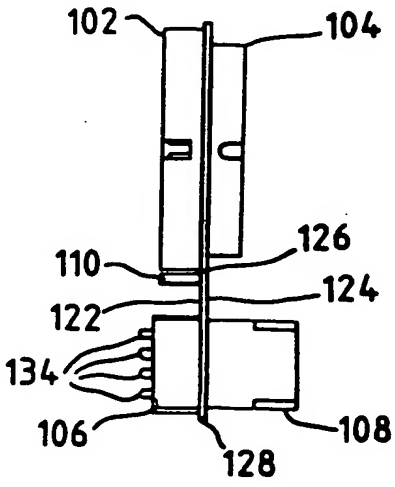

FIG. 10E

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FIG. 11A

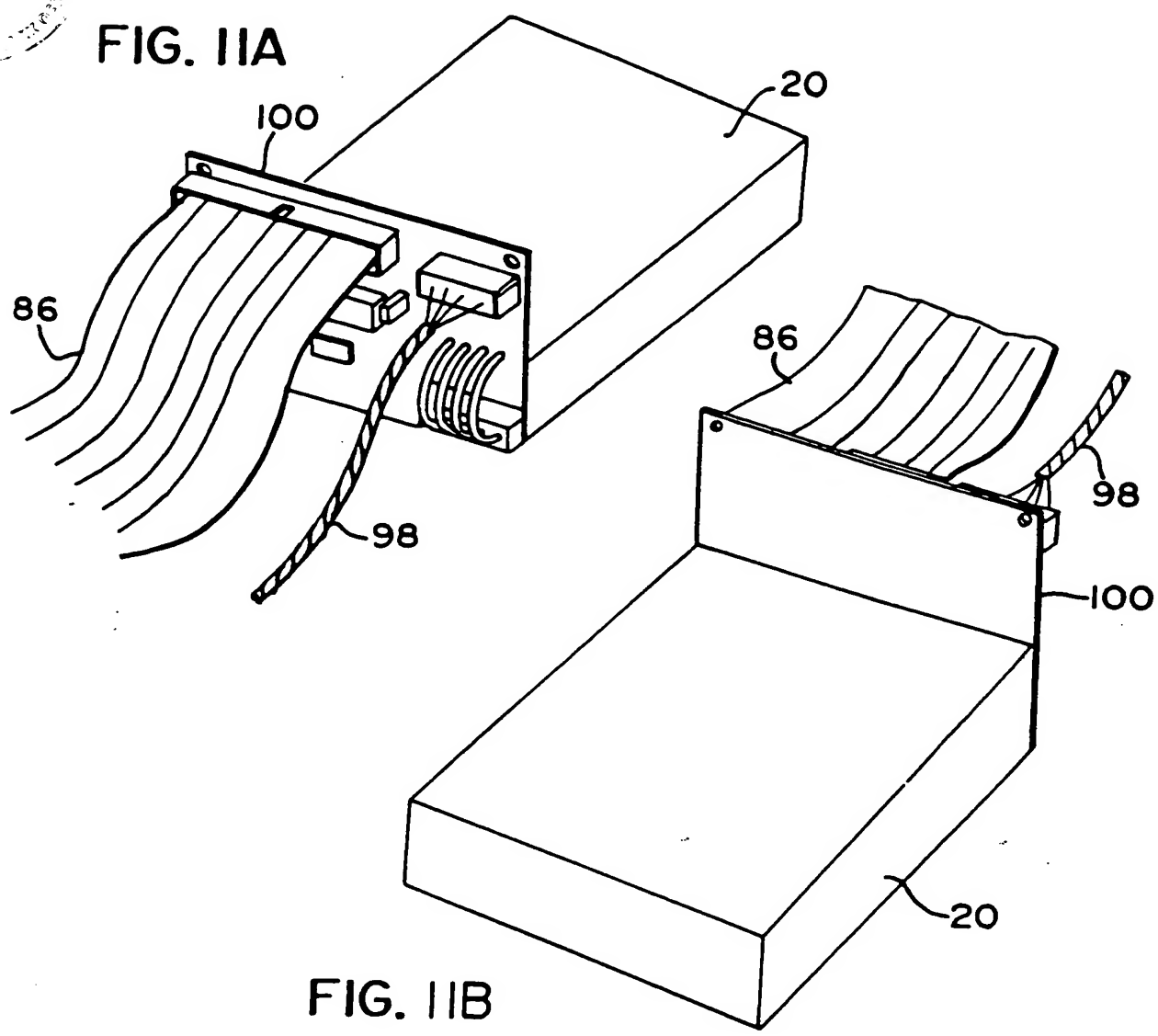

FIG. 11B

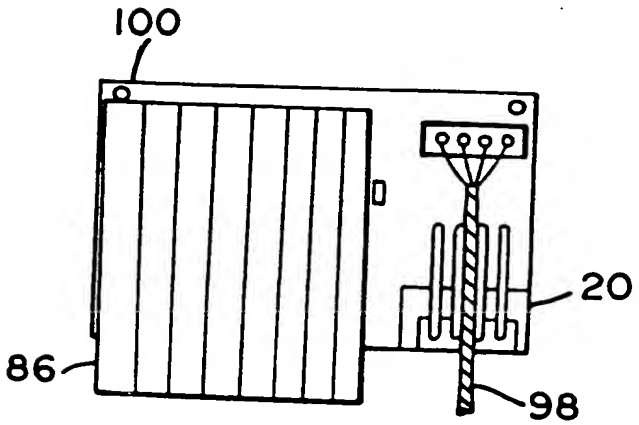

FIG. 11C

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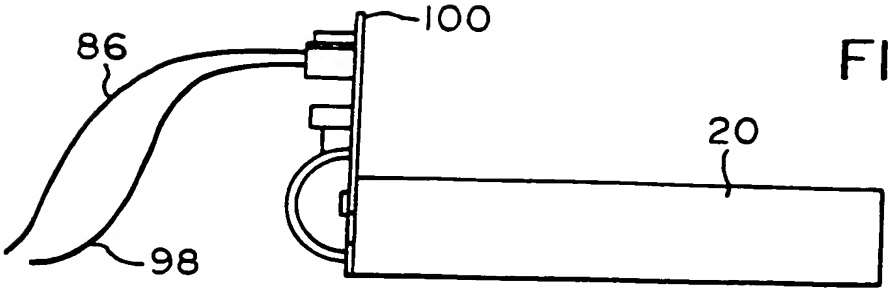

FIG. 11D

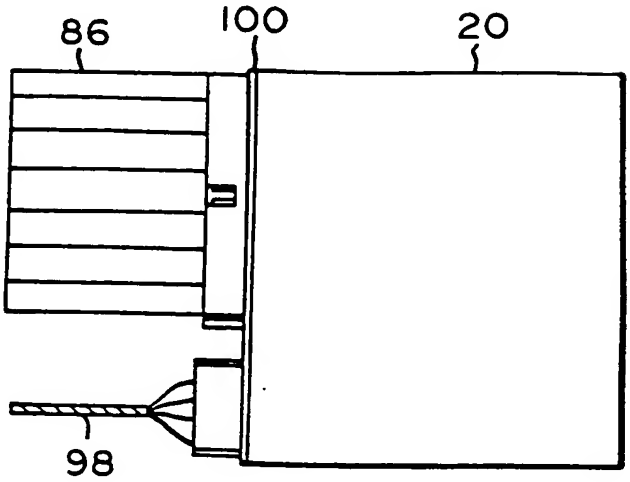

FIG. 11E

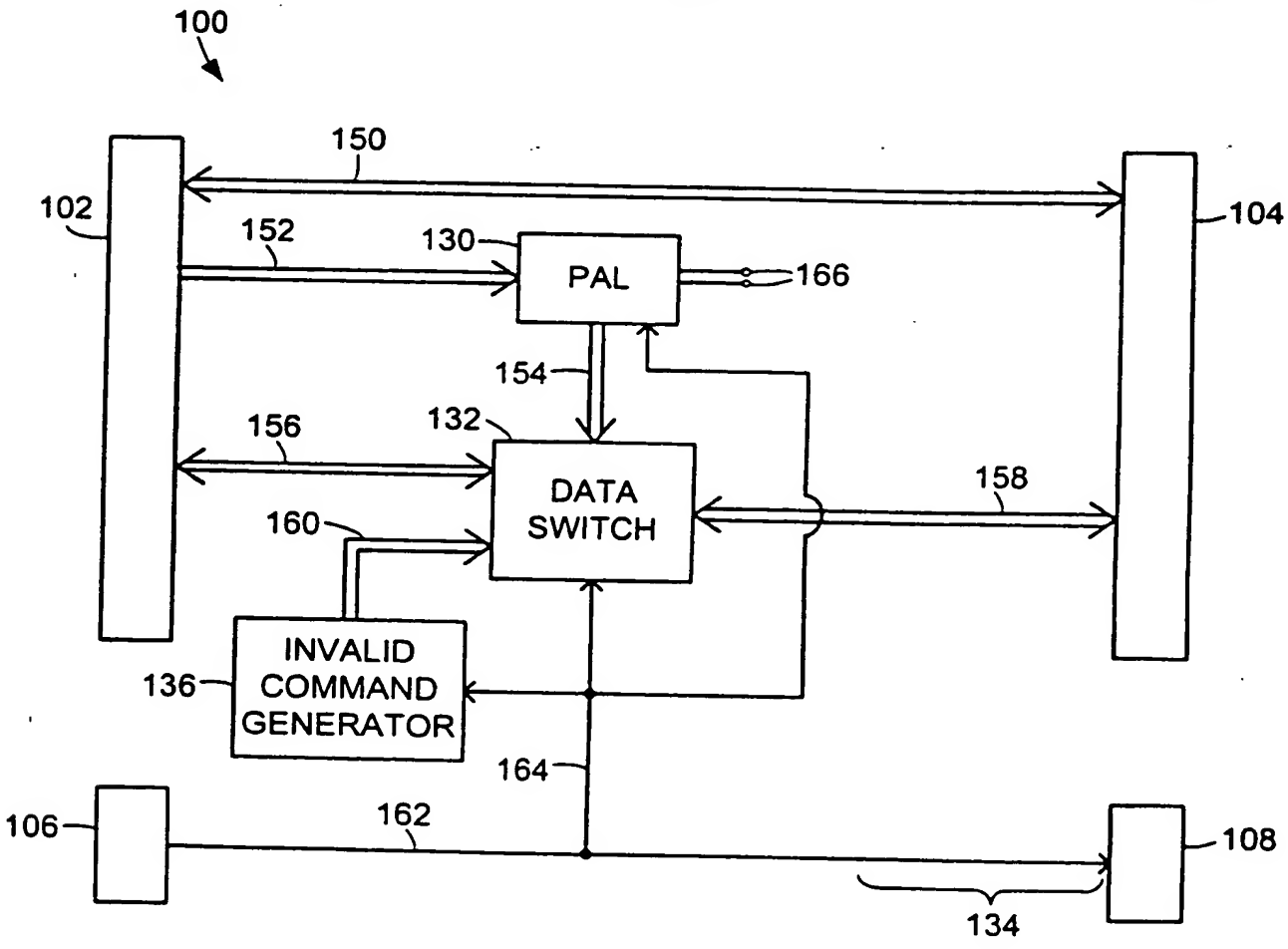

FIG. 12

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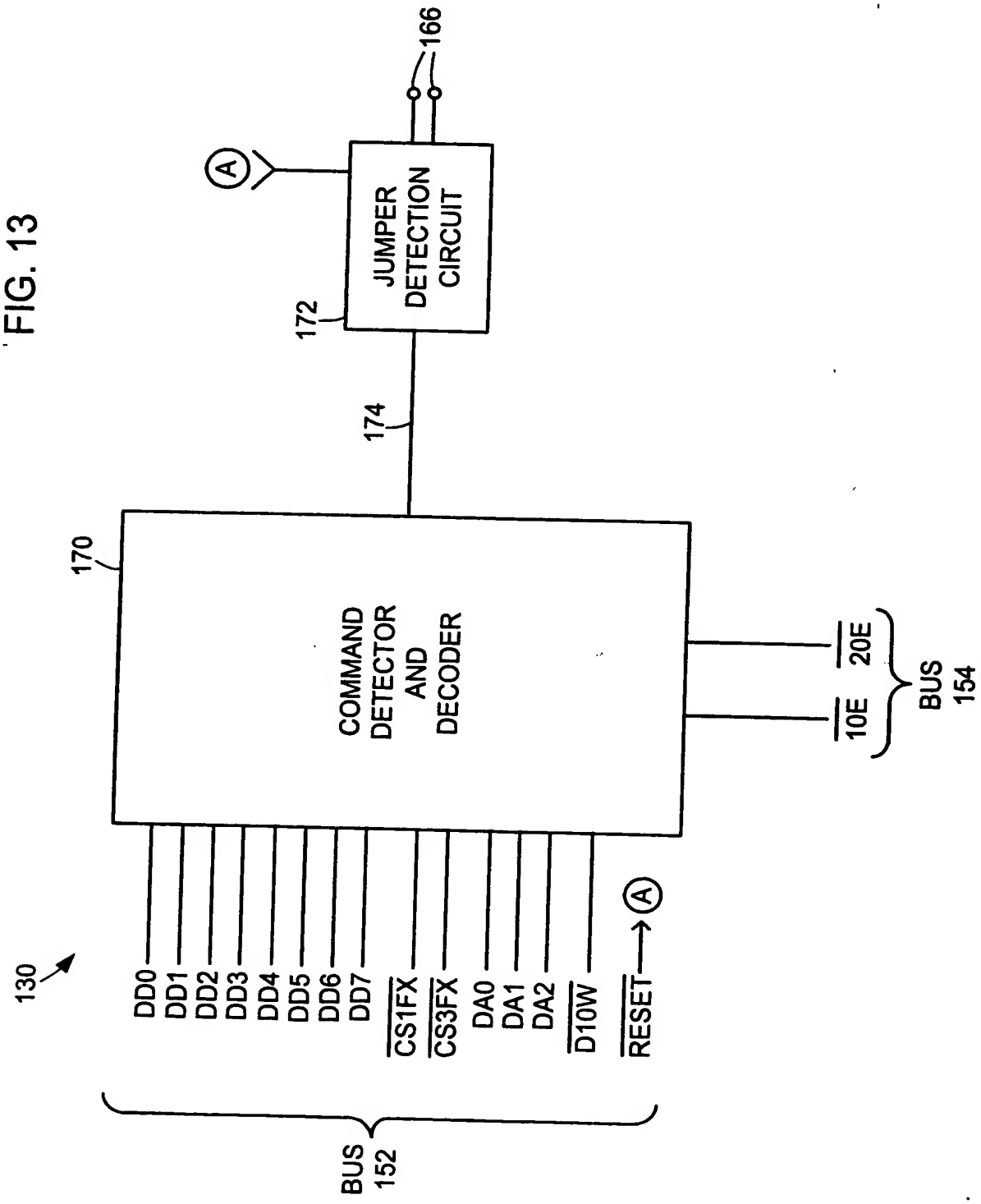
FIG. 13



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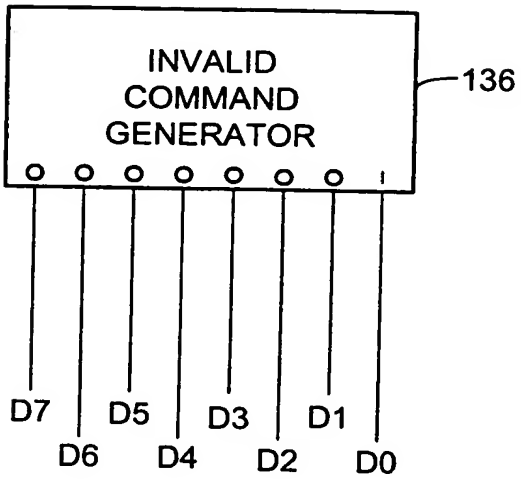

FIG. 14

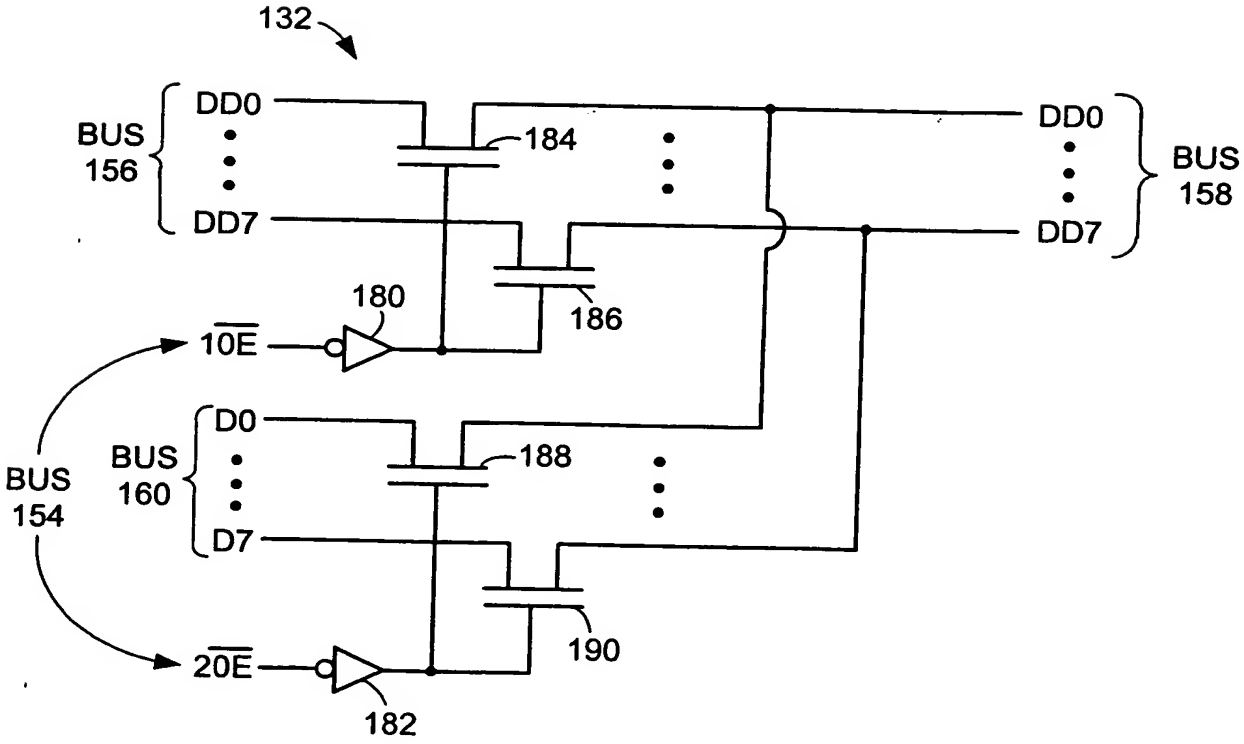

FIG. 15

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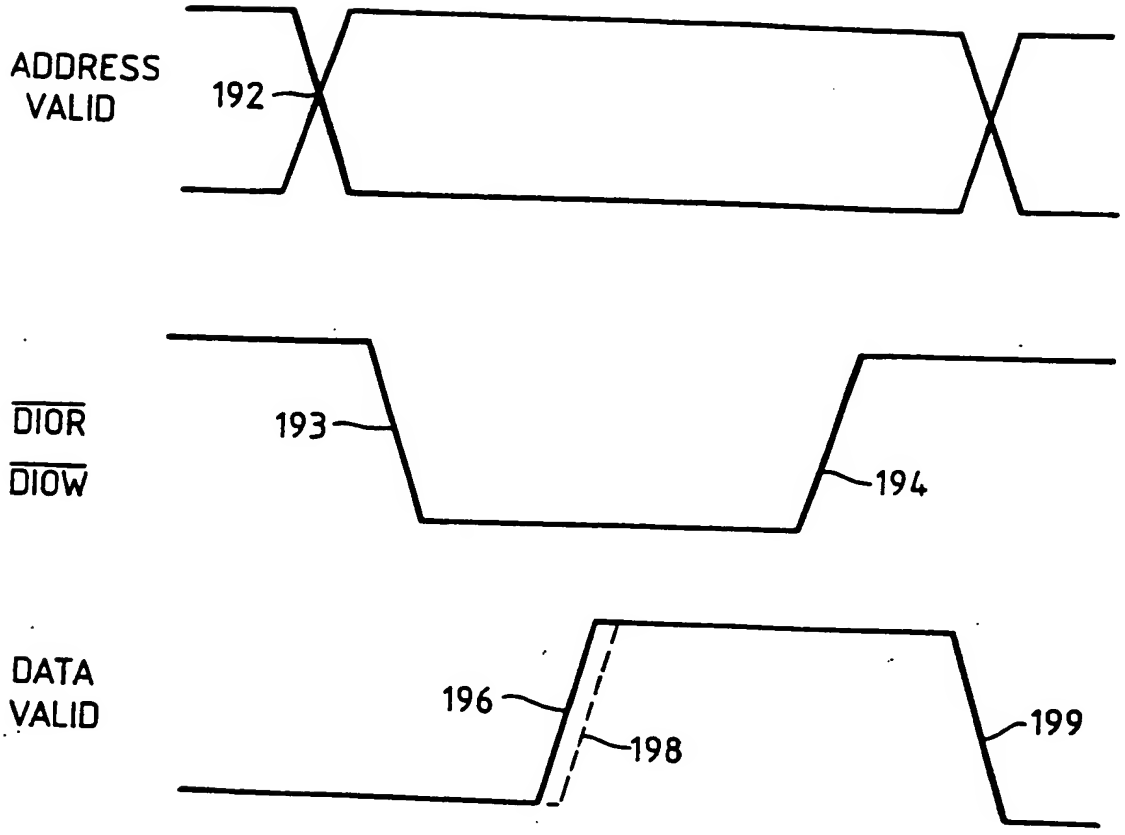

FIG. 16

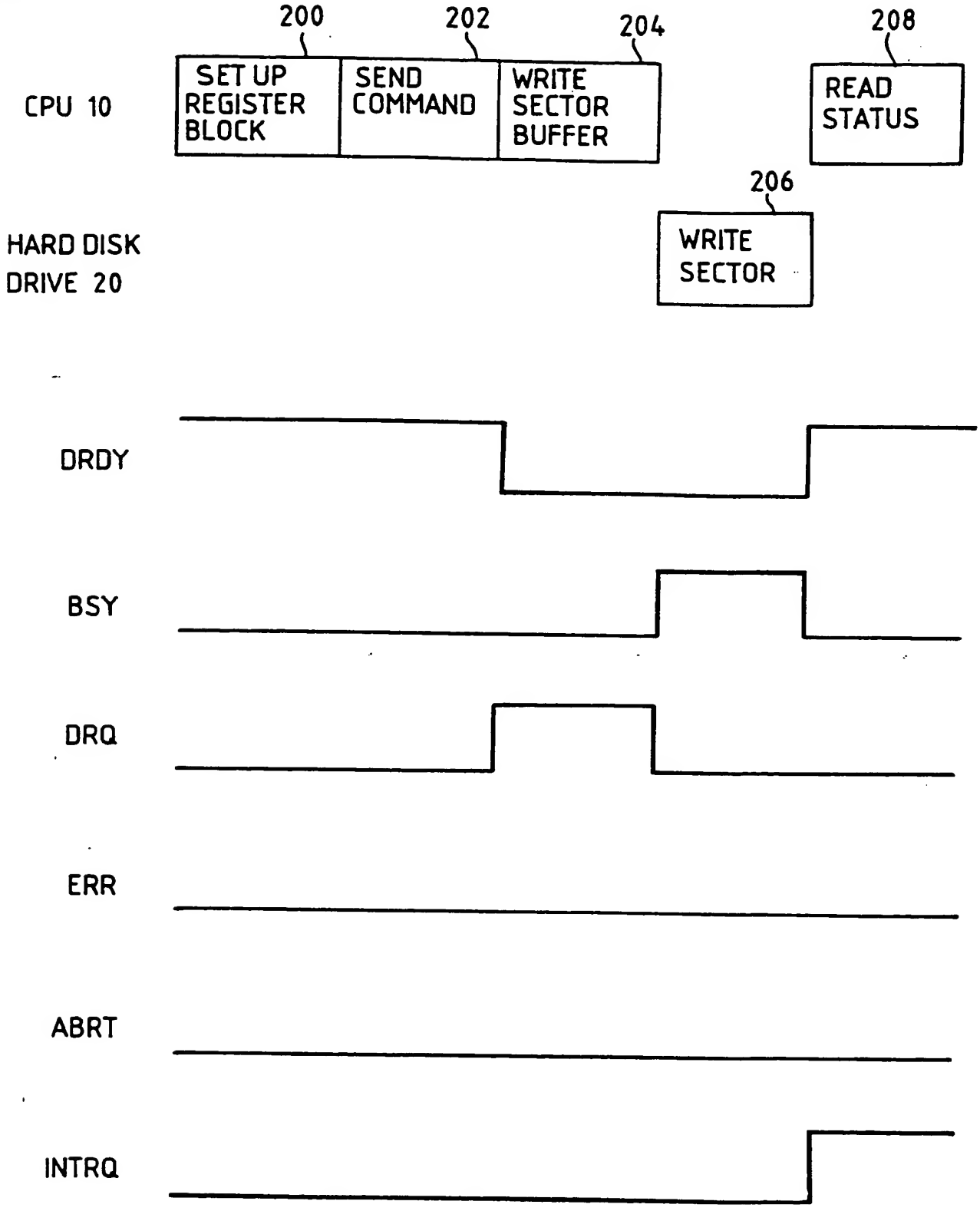
200
202
204
208
CPU 10
SET UP REGISTER BLOCK
SEND COMMAND
WRITE SECTOR BUFFER
READ STATUS
206
HARD DISK DRIVE 20
WRITE SECTOR
DRDY
BSY
DRQ
ERR
ABRT
INTRQ

FIG. 17

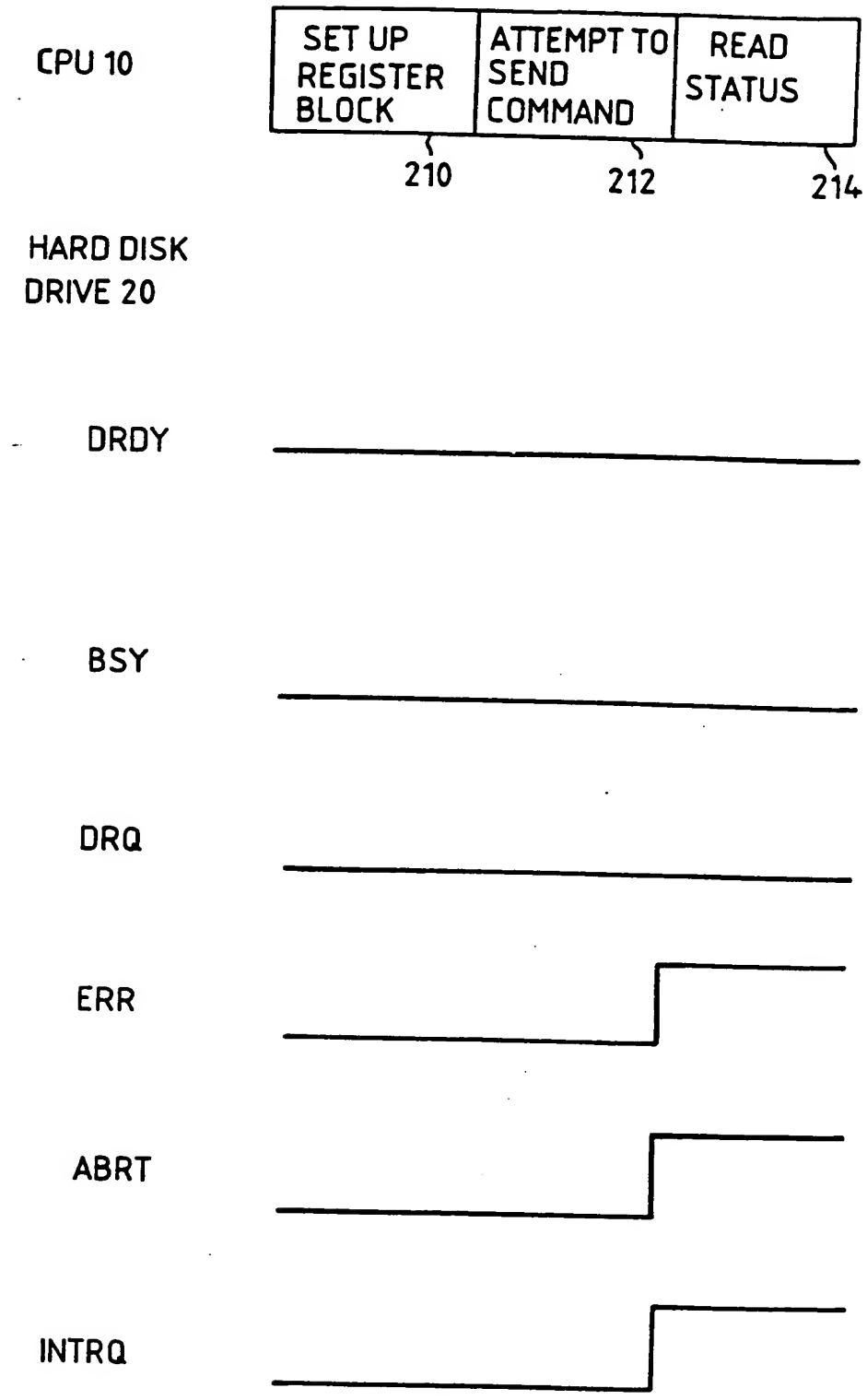
CPU 10
SET UP REGISTER BLOCK
ATTEMPT TO SEND COMMAND
READ STATUS
210
212
214
HARD DISK DRIVE 20
DRDY
BSY
DRQ
ERR
ABRT
INTRQ

FIG. 18

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FIG. 19

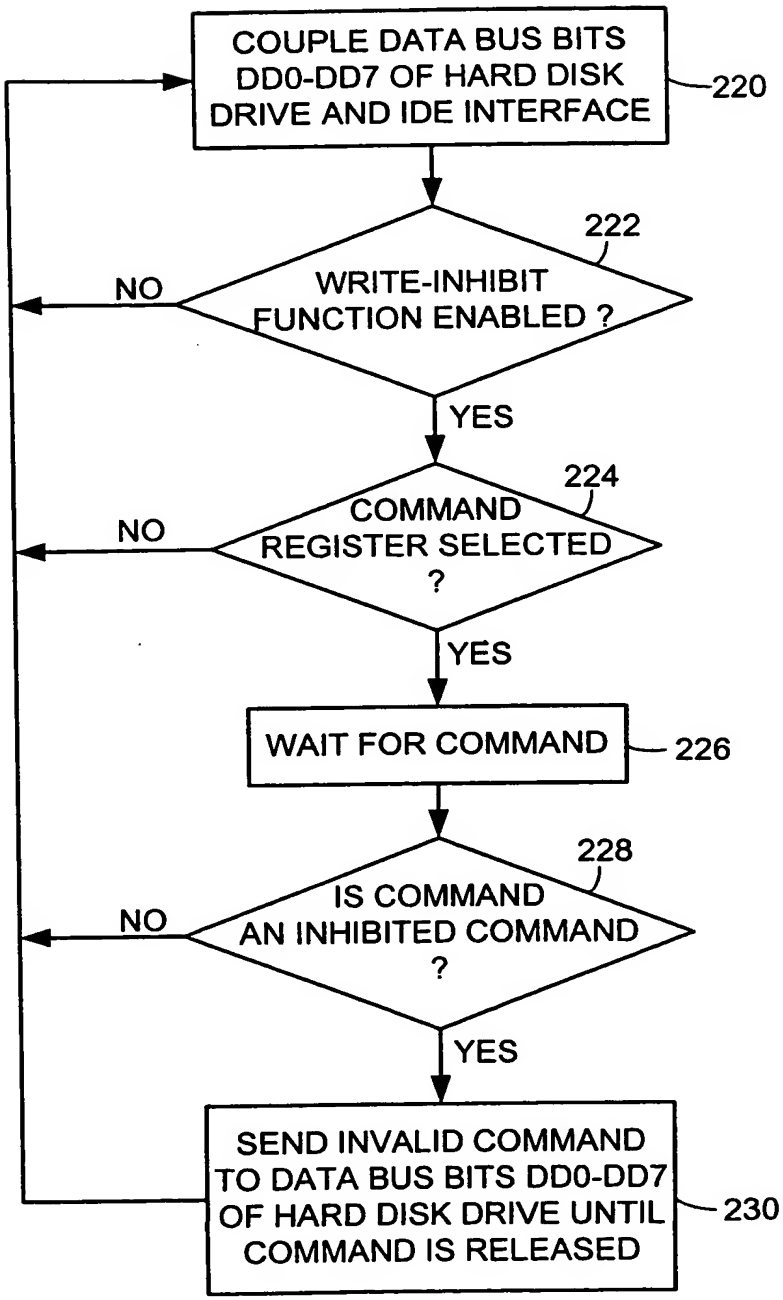

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FIG. 20A

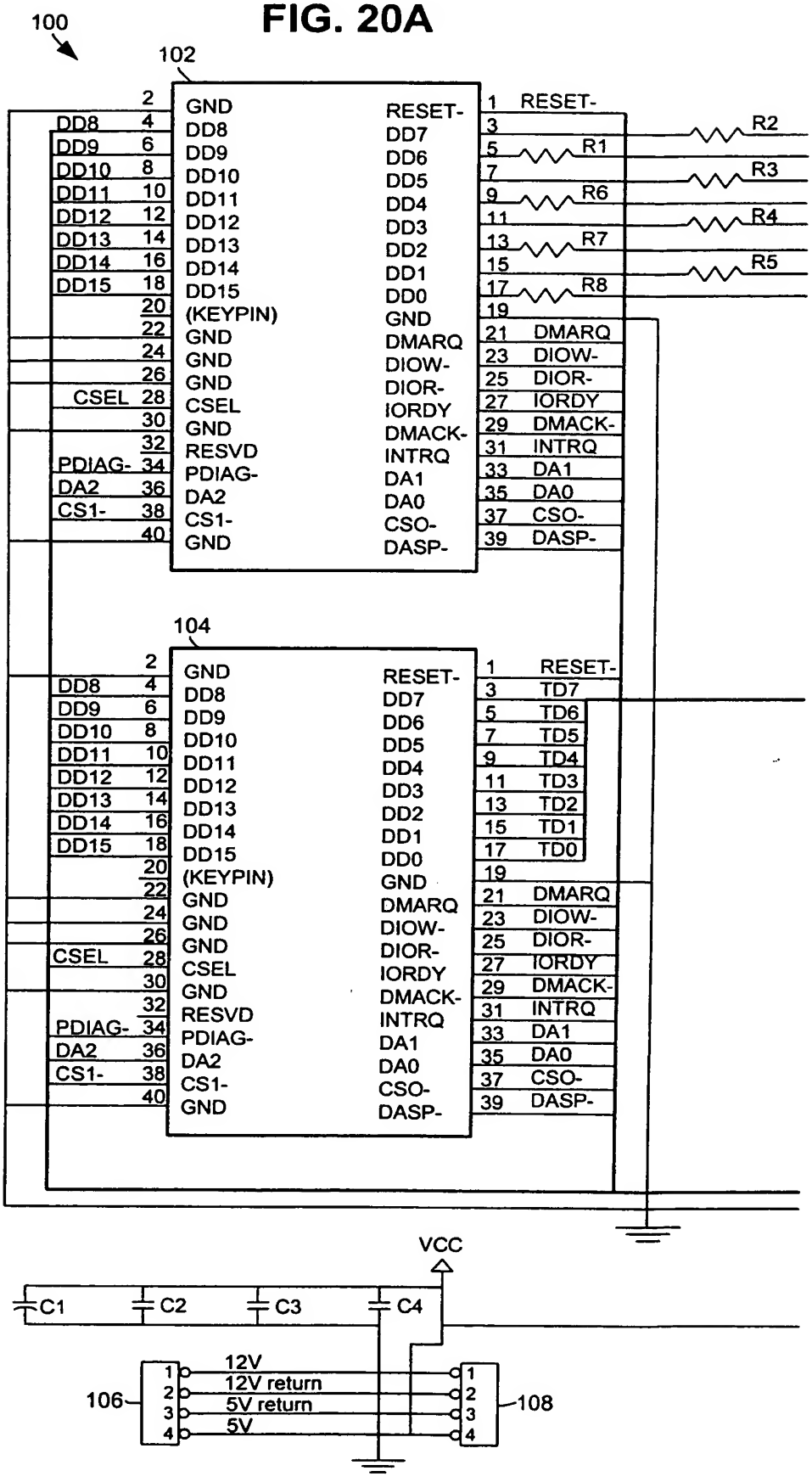
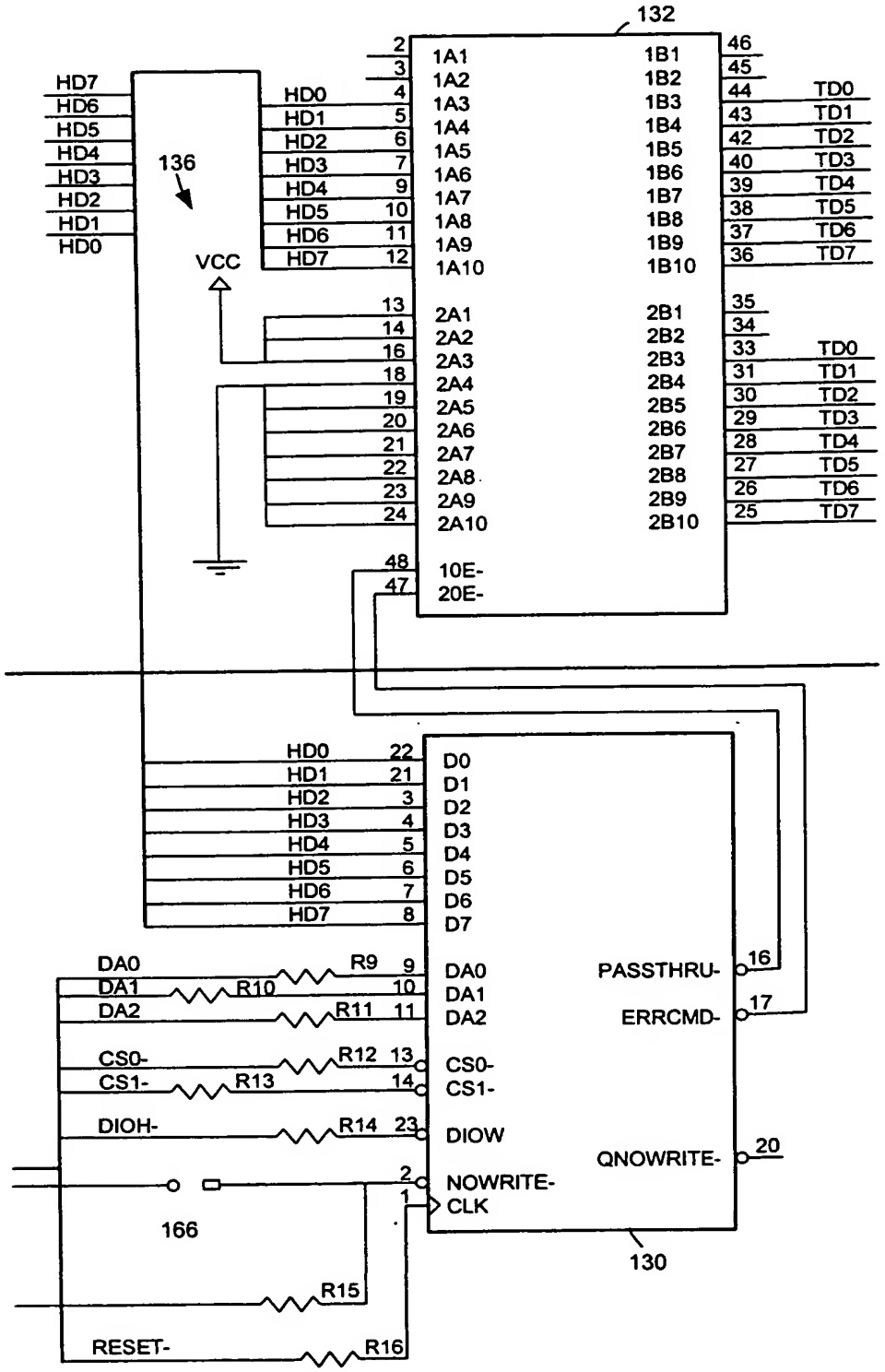


FIG. 20B


132
HD7
HD6
HD5
HD4
HD3
HD2
HD1
HD0
136
VCC
1A1
1A2
1A3
1A4
1A5
1A6
1A7
1A8
1A9
1A10
1B1
1B2
1B3
1B4
1B5
1B6
1B7
1B8
1B9
1B10
TD0
TD1
TD2
TD3
TD4
TD5
TD6
TD7
2A1
2A2
2A3
2A4
2A5
2A6
2A7
2A8
2A9
2A10
2B1
2B2
2B3
2B4
2B5
2B6
2B7
2B8
2B9
2B10
10E-
20E-
D0
D1
D2
D3
D4
D5
D6
D7
DA0
DA1
DA2
R9
R10
R11
CS0-
CS1-
R12
R13
DIOH-
R14
DIOW
NOWRITE-
CLK
PASSTHRU-
ERRCMD-
QNOWRITE-
166
R15
RESET-
R16
130

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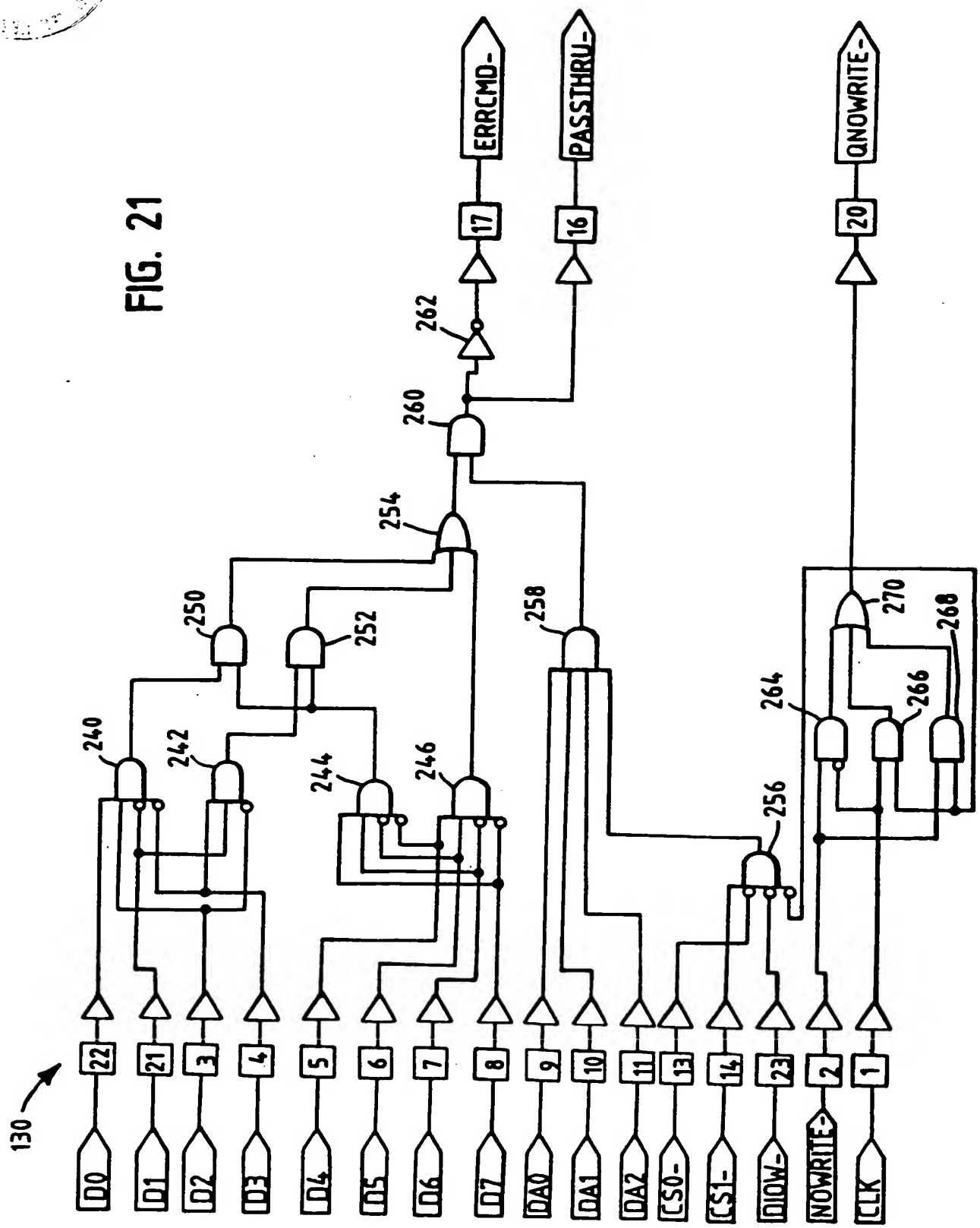
FIG. 21